Pronghorn SBC Hardware Manual

Single/Dual Radio Wireless Router Board

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FCC STATEMENT

The Pronghorn SBC Wireless Router Board has been tested and found to comply with the specifications for a Class B digital device, pursuant to Part 15 of the FCC Rules. Operation is subject to the following two conditions:
(1) This device may not cause harmful interference, and
(2) This device must accept any interference received, including interference that may cause undesired operation.

These limits are designed to provide reasonable protection against harmful interference in a residential installation. This equipment generates, uses, and can radiate radio frequency energy and, if not installed and used according to the instructions, may cause harmful interference to radio communications. However, there is no guarantee that interference will not occur in a particular installation. If this equipment does cause harmful interference to radio or television reception, which is found by turning the equipment off and on, the user is encouraged to try to correct the interference by one or more of the following measures:

- Reorient or relocate the receiving antenna
- Increase the separation between the equipment or devices
- Connect the equipment to an outlet other than the receiver's
- Consult a dealer or an experienced radio/TV technician for assistance

FCC Caution: Any change or modification to the product not expressly approved by ADI Engineering could void the user's authority to operate the device.

Revisions

Date	Revision	Page-paragraph	Remarks
30 July 07	1.00	All	New Document

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1 Introduction

This user manual is a technical overview of the ADI Engineering Pronghorn SBC Wireless Router Board based on the Intel IXP42x network processor. This document is intended primarily for software developers, system integrators or OEMs developing their own applications based on Pronghorn SBC.

Pronghorn SBC is available in a number of different hardware configurations as a single or dual MiniPCI slot wireless router board targeting applications such as WISP infrastructure or CPEs, single or dual radio mesh nodes, hotspot controllers, and OEM applications for high-performance specialized access points. Pronghorn SBC offers a number of unique features that set it apart from competitive boards on the market:

- When used with the ADI RM1 MiniPCI radio, Pronghorn SBC offers an easy path to FCC compliance with real-world high-gain antennas used by WISPs and muni network operators.
- 802.3af compliant PoE with 1500VRMS electrical isolation for compliance with the EN60950 electrical safety standard, and greatly reduced susceptibility of the board to surges and noise emissions.
- 6.5W of continuous MiniPCI power availability at any combination of 3.3V and 5V allows use of even the highest power MiniPCI radios (Note: In dual MiniPCI slot versions, 6.5W per slot cannot be obtained when using 802.3af compliant PoE injectors, due to power limitations of the 802.3af spec. In these cases, a passive PoE injector with sufficient power capacity should be used).
- Extended temperature version built with 100% extended temperature certified components is available (contact ADI for details).
- Extremely quiet design uses spread spectrum clocking of the CPU, I/O and memory busses to reduce peak noise emissions by up to 10dB compared to competitive products. Pronghorn SBC is so quiet it easily passes FCC Part 15 Class B noise emissions standards without an enclosure or shielding or filtering of I/O lines of any sort.

Pronghorn SBC can be mounted in off-the-shelf indoor plastic enclosures or outdoor cast aluminum NEMA rated enclosures. Pronghorn SBC is the basis of ADI Engineering's MeshLink™ wireless CPE device with a flexible configuration of one or two radios.

2 Platform Overview

The Pronghorn SBC has all the components of a typical enterprise 802.11 access point including the interface for LAN, and WAN. The 802.11 WLAN connectivity is achieved through industry standard Mini PCI expansion cards. The board block diagram is shown below in Figure 1.

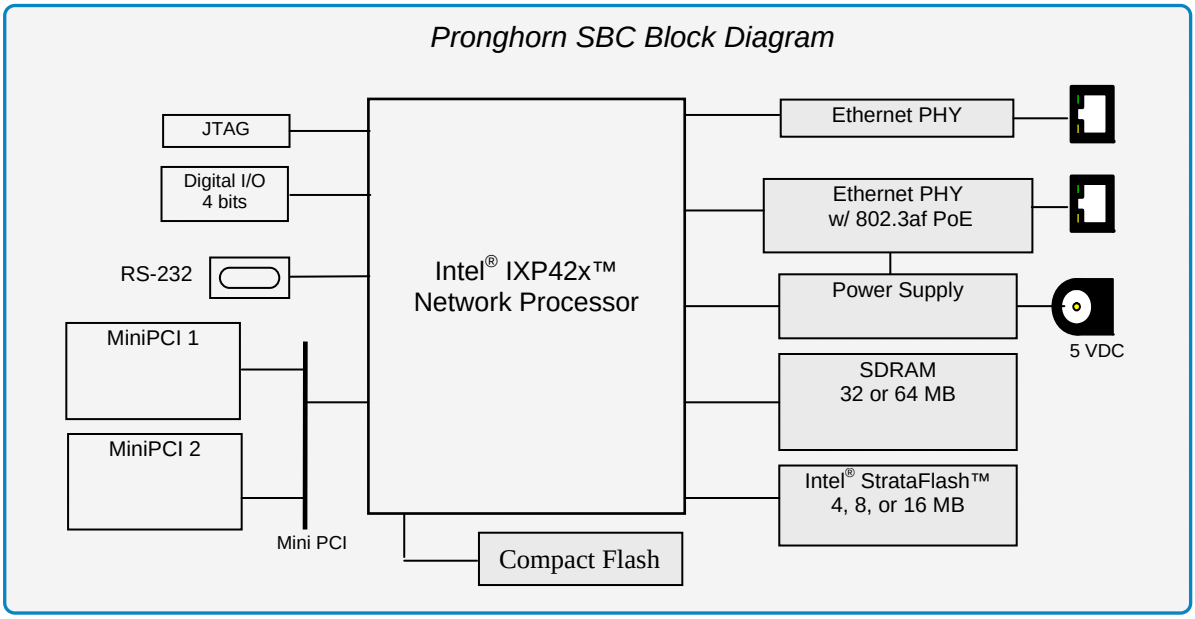

Figure 1. Pronghorn SBC Block Diagram

Standard production versions of Pronghorn SBC, with the associated hardware configurations are detailed in Table 1.

Table 1. Pronghorn SBC Standard Versions

Feature	SBC-200	SBC-200ELC	SBC-210	SBC-250
CPU	IXP420, 266 MHz	IXP420, 266 MHz	IXP420, 266 MHz	IXP425, 533 MHz
SDRAM	64MB	32MB	32MB	64MB
Boot Flash	4MB	16MB	8MB	16MB
Compact Flash Socket	Yes	No	Yes	Yes
10/100 Ethernet Ports	1	1	1	2
MiniPCI Slots	2	1	2	2

Power Inputs	5V nominal (4.5V-5.5V range) via 2.0mm jack (Special build option: 10V-30V)	5V nominal (4.5V-5.5V range) via 2.0mm jack (Special build option: 10V-30V)	❑ 5V nominal (4.5V-5.5V range) via 2.0mm jack (Special build option: 10V-30V) OR ❑ 48V nominal 802.3af compliant PoE (36-60V range with 1500VRMS electrical isolation)	❑ 5V nominal (4.5V-5.5V range) via 2.0mm jack (Special build option: 10V-30V) OR ❑ 48V nominal 802.3af compliant PoE (36-60V range with 1500VRMS electrical isolation)
RS-232 Ports	3.3V TTL level development port ❑ Not end user accessible ❑ Adapter cable from ADI required to connect to standard PC	3.3V TTL level development port ❑ Not end user accessible ❑ Adapter cable from ADI required to connect to standard PC	❑ One RS-232 via RJ-45 connector (EIA-561) ❑ Optional second RS-232 port for volume orders	❑ One RS-232 via RJ-45 connector (EIA-561) ❑ Optional second RS-232 port for volume orders
Digital I/O	None	None	4 bits ❑ Output: 3.3V TTL, 16mA max current ❑ Input: -0.3V to 3.6V maximum	4 bits ❑ Output: 3.3V TTL, 16mA max current ❑ Input: -0.3V to 3.6V maximum
LEDs	Power, Ethernet 1, WLAN; With lightpipes for use in indoor plastic enclosure	Same as SBC-200, without lightpipes	Same as SBC-200, without lightpipes	Adds Ethernet 2 LED, without lightpipes
Watchdog Timer	Built into CPU	Built into CPU	Built into CPU	Built into CPU
Reset Pushbutton	Reset switch on rear edge of board	Reset switch on rear edge of board	Reset switch on rear edge of board	Reset switch on rear edge of board
Regulatory Certifications	❑ FCC Part 15 Class B ❑ Industry Canada - RSS210, ICES003, NMB003, CNR210 ❑ CE Mark - EN 60950, EN 301 489-1, EN 301 489-17, EN 301 893, EN 300 328, EN 800 836 ❑ RoHS/WEEE compliant	Same	Same	Same
Typical Usage	Mesh CPE	Ultra Low-Cost Wireless CPE	WRAP replacement	High-performance mesh infrastructure

2.1 Processor

Pronghorn SBC is based on either the Intel IXP420 or IXP425 network processors, depending on the version of the board. Clock rate is either 266 MHz or 533 MHz, again depending on the version of the board.

A spread spectrum external 33.333-MHz oscillator (MMD M13050H48M) acts as the input clock signal at OSC_IN of the IXP42x network processor. Spread spectrum clocking of the IXP42x is allowed by Intel, and results in approximately an 8-10 dB reduction of peak noise emissions from the Pronghorn SBC. This is one factor behind the extremely quiet operation of Pronghorn SBC, which allows FCC Part 15 compliance even without an enclosure.

The IXP42x network processor's primary features (as used in Pronghorn SBC) are:

- Intel ® XScale™ Core running at 266 MHz or 533 MHz (depending on SBC model)
- Three NPEs for Layer-2 packet/frame network processing.
- Two 10/100-Mbps, full-duplex IEEE-802.3 MAC's with MII interface (not all SBC models support two actual Ethernet ports)
- Dedicated SDRAM with 32-bit memory interface operating at 133 MHz (equal to system clock frequency)
    - Supports up to two banks, each two chips, of two- and three-cycle CAS latency
    - 13-bit address: Maximum, 256 Mbyte; minimum, 32 Mbyte.
- Expansion Bus
    - 24-bit address
    - 16-bit data
    - Eight chip selects
    - Glueless interface to Intel flash and Motorola- and Intel-mode peripherals
- Two UARTS
    - One fast (921-Kbaud) used for XXXX
    - One standard (230.4-Kbaud) used for OS console monitoring
- PCI 2.2 bus:
    - 32-bit address/data bus
    - 33 and 66 MHz
    - Built-in arbiter supports up to four external bus masters
- GPIOs

A high-level view of the IXP42x network processor is shown in Figure 2. The internal bus is partitioned into two segments and data transactions between the network processing elements and RAM, and CPU may be performed concurrently. The CPU bus is bridged to the system PCI bus. The SDRAM controller can support fast SDRAMs with different organizations.

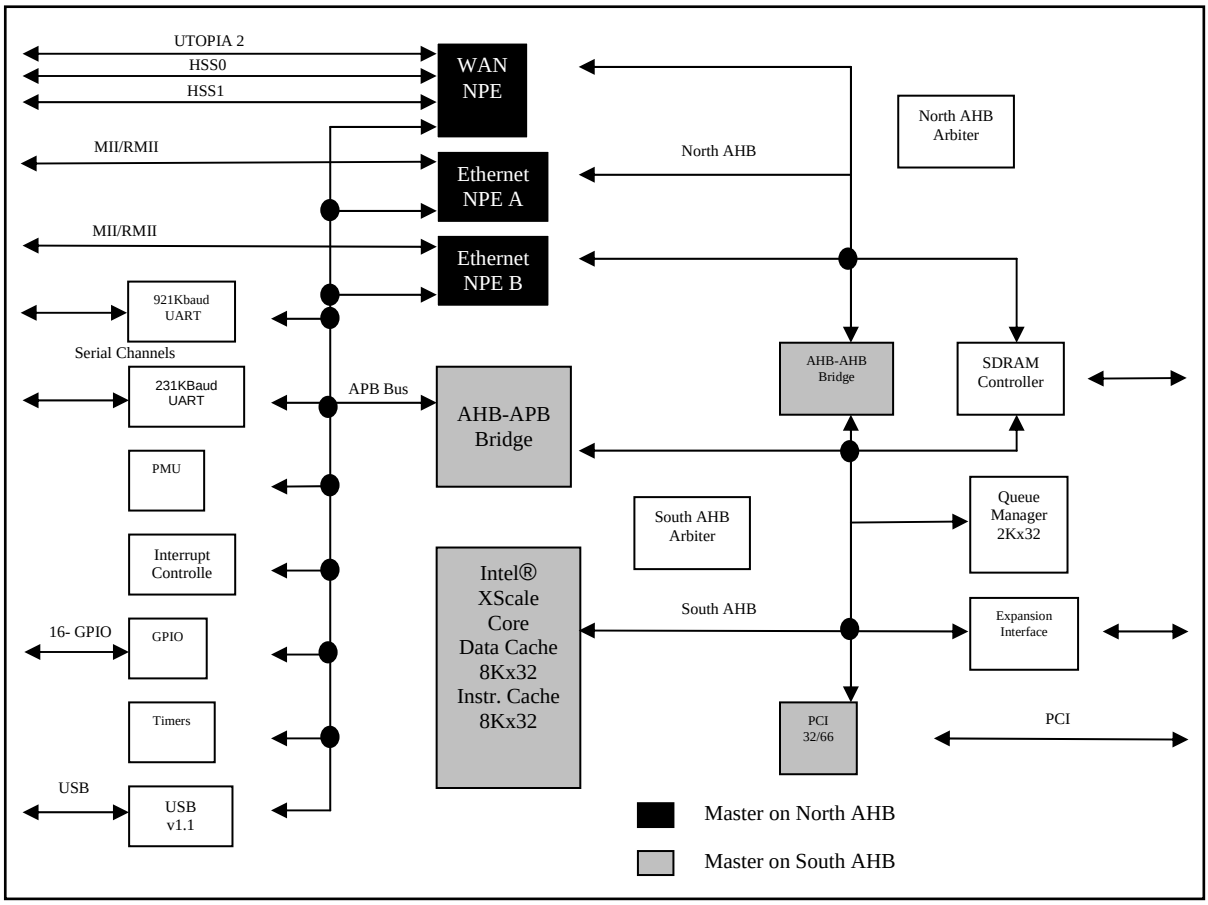

Figure 2. Intel ® IXP42x Network Processor: High-Level View

2.2 Memory Map

The IXP42x network processor implements a single address map that is used for all internal memory and register space. The complete address space consists of 2^32 byte addressable locations.

Table 2. Intel ® IXP42x Network Processor: Memory Map

Start Address	End Address	Size	Description
0000_0000	0FFF_FFFF	256 Mbyte	Expansion-bus data
0000_0000	3FFF_FFFF	1 Gbyte	SDRAM data
4000_0000	47FF_FFFF	128 Mbyte	Reserved
4800_0000	4FFF_FFFF	128 Mbyte	PCI data
5000_0000	5FFF_FFFF	256 Mbyte	Expansion-bus data
6000_0000	63FF_FFFF	64 Mbyte	Queue manager
6400_0000	BFFF_FFFF		Reserved
C000_0000	C000_00FF	256 Mbyte	PCI configuration registers
C000_0100	C3FF_FFFF		Reserved
C400_0000	C400_00FF	256 Mbyte	Expansion-bus configuration registers
C400_0100	C7FF_FFFF		Reserved
C800_0000	C800_0FFF	1 Kbyte	Fast UART (not available on Pronghorn)
C800_1000	C800_1FFF	1 Kbyte	Console UART

C800_2000	C800_2FFF	1 Kbyte	Internal Bus Performance Monitoring Unit (PMU)
C800_3000	C800_3FFF	1 Kbyte	Interrupt controller
C800_4000	C800_4FFF	1 Kbyte	GPIO controller
C800_5000	C800_5FFF	1 Kbyte	Timers
C800_6000	C800_6FFF	1 Kbyte	WAN/HSS NPE – Not user programmable
C800_7000	C800_7FFF	1 Kbyte	Ethernet NPE A – Not user programmable
C800_8000	C800_8FFF	1 Kbyte	Ethernet NPE B – Not user programmable
C800_9000	C800_9FFF	1 Kbyte	Ethernet MAC A (ETH-0)
C800_A000	C800_AFFF	1 Kbyte	Ethernet MAC B (ETH-1)
C800_B000	C800_BFFF	1 Kbyte	USB controller (not available on Pronghorn)
C800_C000	C800_FFFF		Reserved
C801_0000	CBFF_FFFF		Reserved
CC00_0000	CC00_00FF	256 byte	SDRAM configuration registers
CC00_0100	CEFF_FFFF		Reserved
D000_0000	FFFF_FFFF		Reserved

The lowest 256 Mbyte of address space is configurable, based on the value of a configuration register located in the expansion-bus controller. When the configuration register is set to logic 1, the expansion bus occupies the lowest 256 Mbyte of address space. When the configuration register is set to logic 0, the SDRAM occupies the lowest 256 Mbyte of address.

In both cases, the SDRAM occupies the 768 Mbyte immediately following the lowest 256 Mbyte. On reset, the configuration register in the expansion bus is set to logic 1. This setting is required because the dedicated boot memory is flash memory located in the expansion bus.

2.3 SDRAM Memory

The IXP42x network processor supports PC-133-compatible SDRAM with 16-bit-wide devices only. The banks are accessed 32 bits at a time. Pronghorn SBC supports either 16 Mbyte or 32 Mbyte devices, using two chips of a x 16 x 4 banks configuration.

The on-chip IXP42x SDRAM controller is optimized for handling eight-word bursts from the SDRAM. The SDRAM controller throttles the data throughput by controlling the CKE pin of the SDRAM and Wait signal of internal bus.

Byte-handling is performed only for write operations to the SDRAM by controlling the DQM pins of the SDRAM. All read operations are performed by reading the complete bus width of data.

The SDRAM controller has a policy to keep up to eight pages open simultaneously. If a request is received for an open page, the row access (RAS) address cycle is not performed. If the requested page is not currently open, the SDRAM controller first closes the currently open page in that bank, then opens the new page.

2.4 IXP42x GPIO Mapping

IXP42x GPIO pin mappings are as specified in Table 3.

Table 3. IXP42x GPIO Pin Assignments

GPIO	Direction	Function
0	In	Compact Flash Interrupt Request (CF-IRQ)
1	In/Out	DIO0
2	In/Out	DIO1
3	In/Out	DIO2
4	Out	Ethernet 0 Status LED
5	Out	Ethernet 1 Status LED
6	In	MiniPCI B INT# (PCI_INTB) – Bottom side MiniPCI Slot
7	Out	Board Status LED
8	Out	Wireless Status LED
9	In	Compact Flash CD
10	In	DIO3
11	In	MiniPCI A INT# (PCI_INTA) – Top side MiniPCI Slot
12	Out	IO Reset – Software controlled reset of Ethernet PHYs and MiniPCI slots
13	N/A	Unused
14	Out	33-MHz PCI clock (PCI_CLK)
15	Out	33-MHz Expansion bus clock (EXT_CLK)

2.5 Compact Flash

A Compact Flash (CF) socket is provided on Pronghorn SBC. The CF interface operates in True IDE mode, and is physically implemented with a direct connection to the IXP42x expansion bus. CF is operated in Programmed Input/Output (PIO) mode. (Note: The expansion bus does not support DMA.)

IXP42x expansion bus chip selects CS2 and CS3 are used control chip selects “CS0” and “CS1” of the Compact Flash interface, respectively. The interrupt from the Compact Flash is connected to GPIO0. The Compact Flash is reset along with the microprocessor, and it is also reset under software reset control by the I/O Reset signal driven by GPIO12.

GPIO9 is used to sense CD1* on the Compact Flash socket. This GPIO is pulled high with a resistor on Pronghorn SBC. When a Compact Flash card is installed, it connects CD1* to ground. Software can detect the presence of a Compact Flash by checking if GPIO9 is a logic low. If GPIO9 is a logic high, no Compact Flash card is installed.

2.6 Expansion Bus Chip Select Assignments

The chip selects of Pronghorn SBC devices that are connected to the expansion bus are listed in Table 4.

Table 4. IXP42x Expansion Bus Chip Select Assignment

Chip Select	Assignment
CS0	Flash 0
CS1	Flash 0
CS2	Compact Flash CS0
CS3	Compact Flash CS1
CS4-CS7	Not Used

Note: CS0 and CS1 are connected to one StrataFlash device (Flash 0) that is partitioned onto two chip selects. This is required for potential expansion of the StrataFlash to 256Mbit density.

2.7 Digital I/O

The Pronghorn SBC-210 and 250 offer four bits of 3.3V TTL level user-defined digital I/O (DIO) available on connector J16. These DIO bits are intended to connect low-power I/O devices to the Pronghorn SBC – tamper detect switches, auxiliary control boards, smart antenna controllers, and so on. The DIO lines are ESD protected, but are not electrically isolated and do not have protection against sustained overloads, so they should not be used for out-of-cabinet applications that may be subjected to these conditions.

IXP42x GPIO lines are used to provide DIO functionality, as listed in Table 5. Table 4 also specifies the pinout of connector J16. All DIO lines are pulled to 3.3V with 4.7 kohm resistors on Pronghorn SBC. Ground and 3.3V pins are available on J16 to facilitate connection with open-drain drivers, or electromechanical devices such as switches or relays.

The maximum input voltage range for DIO bits configured as inputs is -0.3V to +3.6V. Maximum output current when configured as outputs is 16mA.

Application of voltages outside this range may result in damage to the Pronghorn SBC.

Table 5. DIO-GPIO Mapping; J16 Pin Assignments

DIO Line	IXP42x GPIO Assignment	J16 Pin Assignment
DIO0	GPIO1	1
DIO1	GPIO2	3
DIO2	GPIO3	5
DIO3	GPIO10	7
		3.3V – Pin 9
		Ground – Pins 2, 4, 6, 8, 10

2.8 StrataFlash

The boot ROM of Pronghorn is a single Intel StrataFlash ® J3D device connected through the expansion bus. StrataFlash densities supported are 4MByte, 8MByte and 16MByte, depending on the version of the Pronghorn SBC.

Multiple images may be written into the flash. The boot image is chosen by changing the location of the boot address determined by the BSP from bits [20:17] of the processor configuration register 0. These bits are programmed with shorting bars on J12, which strap the expansion bus address bits [20:17] to a logic zero. Following power-up or reset, the logic values on expansion bus address bits [20:17] are transferred to configuration register 0. Bit [20] selects between the two flash devices and bits [19:17] represent the high-order three bits (address line 23, 22 and 21) of the expansion address bus. The process boot code reads the states of the bits and calculates the start address for the boot. With these three bits, each flash can boot from one of eight address locations.

The size of the data transfer to StrataFlash is set to 16 bits for Pronghorn SBC.

2.9 MiniPCI Interface

The Pronghorn SBC supports one or two Mini PCI connectors (depending on model) with the PCI interface on the IXP42x chip configured as a PCI host. Pronghorn SBC offers several high-performance characteristics for the MiniPCI interfaces:

- 6.5W continuous power availability per slot, at any combination of 3.3V and 5V
- Ability to power even the highest power radios with ease – Ubiquiti XR series, Wavesat MiniPCI, etc.
- Ability to handle elongated MiniPCI cards

The details of the Mini PCI interface include:

- Chip Select — PCI_REQ1 and PCI_GNT1 for slot 1 (top side) and PCI_REQ2 and PCI_GNT2 for slot 2 (bottom side)
- Interrupts — GPIO 11 and GPIO6, active low, as PCI-IRQAn and PCI_IRQBn, respectively
- Clock — GPIO 14
- Software controlled reset — GPIO 12, active low

As the IXP42x network processor is the PCI host, reset will be driven to the PCI devices from the system reset circuit.

The PCI_IDSEL pin on the processor is pulled up to 3.3 V. The IDSEL's on the Mini PCI slots are connected to PCI_AD17 and PCI_AD18 for slots 1 and 2 respectively, giving each a unique device number on the PCI bus.

2.10 Ethernet Interfaces

- Interface: MDC/MDIO
  - Programmed reset: GPIO 12, active low

- Interface: Ethernet 0 to primary Ethernet port (ETH)
  - Clock: External, 25 MHz

- Interface: Ethernet 1 to secondary Ethernet port (ETH 2)
  - Clock: External, 25 MHz

The IXP42x network processor has two Ethernet 10/100BaseT interfaces, implemented with Ethernet coprocessors built into the NPEs. The coprocessors provide support for MII and RMII interfaces to the external PHY. They support both full-duplex and half-duplex mode of operation and also contain two 256-byte FIFO: one for transmit data and the other for receive data.

The processor includes a single management data interface — Management Data Input Output (MDIO) — and Management Data Clock (MDC) to program the Ethernet PHYs.

On Pronghorn SBC, the two Ethernet ports are directly connected to the Ethernet controller via the MII interface and PHY chips as shown in Figure 3.

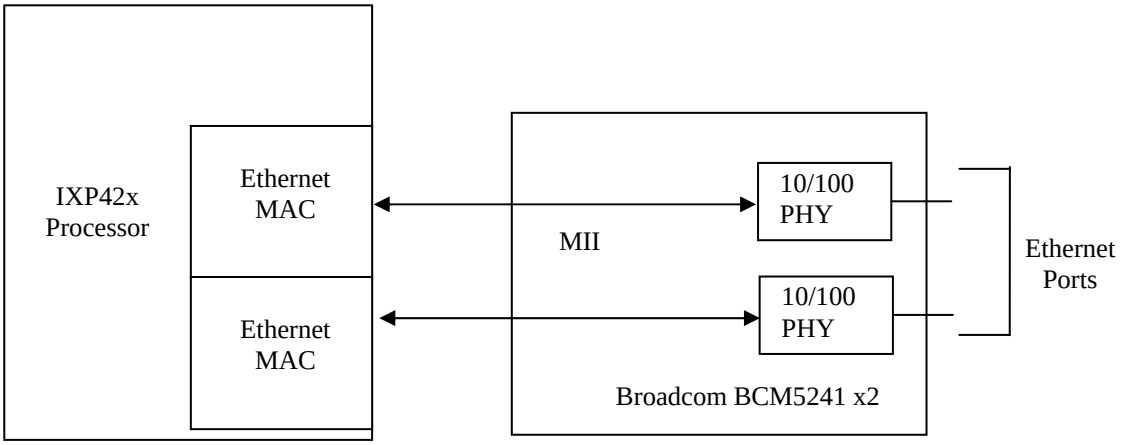

Figure 3. Implementation of Ethernet Ports

2.11 Serial Ports

The IXP42x network processor provides two dedicated asynchronous, serial, I/O ports (UART0 and UART1). These UARTs are 16550-compliant with flow control and enhanced with larger 64-byte transmit and receive buffers.

Pronghorn SBC uses these two UARTs to provide two serial ports. Exact configuration of the serial ports varies by the specific Pronghorn SBC model number.

Serial port 1 is an RS-232 port available via RJ-45 connector J9. Serial port 2 is a special order option from ADI and is available via RJ-45 connector J8. Both J8 and J9 follow the EIA-561 standard for RS-232 over RJ-45 connectors. Pinout of J8 and J9 is specified in Table 6.

WARNING: *Do not connect an energized PoE injected Ethernet cable to J8 or J9. Permanent damage to the Pronghorn SBC may result.*

Pronghorn SBC-200 and 200ELC do not have J9 and the associated RS-232 level translators. For these boards, Serial Ports 1 and 2 are available not as a user-accessible ports, but rather as board test and configuration interfaces for use during board integration and provisioning via J12. This connector offers the serial ports as 3.3V TTL level (NOT RS-232 level) interfaces and pinout is as specified in Table 7. A special RS-232 adapter cable is required from ADI to connect J12 to a standard RS-232 port on a host PC.

Table 6. J8 and J9 RJ-45 Serial Port Connector Pinouts

Pin Number	Signal Name	Pin Number	Signal Name
1	NC	2	NC
3	NC	4	GND
5	TXD	6	RXD
7	RTS	8	CTS

Table 7. J12 Serial Port Connector Pinout (3.3V TTL Level)

Pin Number	Signal Name	Pin Number	Signal Name
1	GND	2	3.3V
3	URT1_RXD	4	URT1_TXD
5	URT2_RXD	6	URT2_TXD

2.12 IXP42x JTAG Interface

Pronghorn SBC includes an ARM-standard 20-pin JTAG header for use with IXP42x emulators and debuggers. The Pronghorn SBC 200 and 210 are intended for very low-cost, high-volume CPE applications and they do not include the JTAG connector in order to save the cost of an unused feature.

Pronghorn SBC's JTAG port is compatible with any of the available third-party XScale JTAG tools, from vendors including Macraigor Systems, Abatron, Embedded Performance, ARM, and others.

The Pronghorn reset circuit requires that the JTAG reset be open drain and active low. It is wire OR'ed with push-button reset and power-on reset to generate a reset to the processor.

Table 8. JTAG Connector Pinout

Pin #	Pin Name	Connect To	Pin #	Pin Name	Connect To
1	VTREF	+3.3V	2	VSUPPLY	+3.3V
3	TRST_N	JTG_TRST 10-K Ω pull-down – TRST also generated from reset circuit whenever system reset asserted and from Corelis test equipment	4	GND	GND
5	TDI	JTG_TDI	6	GND	GND
7	TMS	JTG_TMS 10-K Ω pull-up	8	GND	GND
9	TCK	JTG_TCK 10-K Ω pull-up	10	GND	GND
11	RTCK	GND	12	GND	GND
13	TDO	JTG_TDO	14	GND	GND
15	SRST_N	Reset circuitry	16	GND	GND
17	DBGRQ	Not Connected	18	GND	GND
19	DGBACK	Not Connected	20	GND	GND

2.13 Indicator LED's

Pronghorn SBC has a total of four sites for indicator LEDs, as shows in Table 9. Please note that as supplied by ADI, the Status, Wireless, Ethernet, and Ethernet 2 LED's are driven by hardware automatically and are not software controllable. However for volume orders, ADI can custom configure these LEDs as being under software control.

Table 9. Pronghorn SBC LED's

LED	Description
LD1	Ethernet 1 (J7) Link/Activity. Driven directly by BCM5241 PHY. Solid green indicates link; Blinking indicates activity. Optionally, LD1 can be factory configured to be driven by IXP42x GPIO5. Minimum purchase quantities required for this custom configuration.
LD2	Ethernet 0 (J6) Link/Activity. Driven directly by BCM5241 PHY. Solid green indicates link; Blinking indicates activity. Optionally, LD2 can be factory configured to be driven by IXP42x GPIO4. Minimum purchase quantities required for this custom configuration.
LD3	Driven by pin 11 of the J3 (topside) MiniPCI slot – usually indicates radio card active. Optionally, LD3 can be factory configured to be driven by IXP42x GPIO8. Minimum purchase quantities required for this custom configuration.
LD4	Driven by IXP42x GPIO7. Redboot turns ON shortly after power up – indicates power present and software operational

2.14 Platform Reset Circuitry

The board generates a power-on reset upon the required voltages reaching valid levels. Power-on reset signal resets all the circuitry.

A reset switch provided on the board also resets the entire board. Additionally GPIO 12 (as an active-low signal) drives a software-controlled reset of the Ethernet PHYs and MiniPCI slots.

2.15 Power Input Options

The input power to the platform is obtained through one of two interfaces: 802.3af compliant Power over Ethernet on the primary Ethernet port (J6) or the barrel connector power input (J10). The PoE input conforms to the 802.3af specification, and therefore requires 48V nominal (36-60V range). The input voltage range on J10 is 4.5V – 5.5V.

ADI also offers as a special build configuration (subject to minimum order quantities) a 10V-30V wide-range input for J10. Please contact your ADI reseller for pricing and availability.

Note that the 802.3af specification does not allow for sufficient power to accommodate Pronghorn SBC with two 6.5W MiniPCI radios. This situation is easily solved by using a passive PoE injector with a 20W or greater power supply when powering a fully-loaded Pronghorn SBC.

1500VRMS of electrical isolation is designed into the PoE regulators on Pronghorn SBC, in compliance with EN60950 electrical safety specification. The barrel connector does not offer electrical isolation, however.

2.16 Mechanical

The Pronghorn SBC printed circuit board has a mechanical form factor as show in Figure 4. The board fits into a wide variety of off-the-shelf enclosures including the following:

- Pacific Wireless DCE NEMA 6 cast aluminum
- Pacific Wireless Rootenna
- Polycase AG-85 low-cost plastic indoor
- Many others

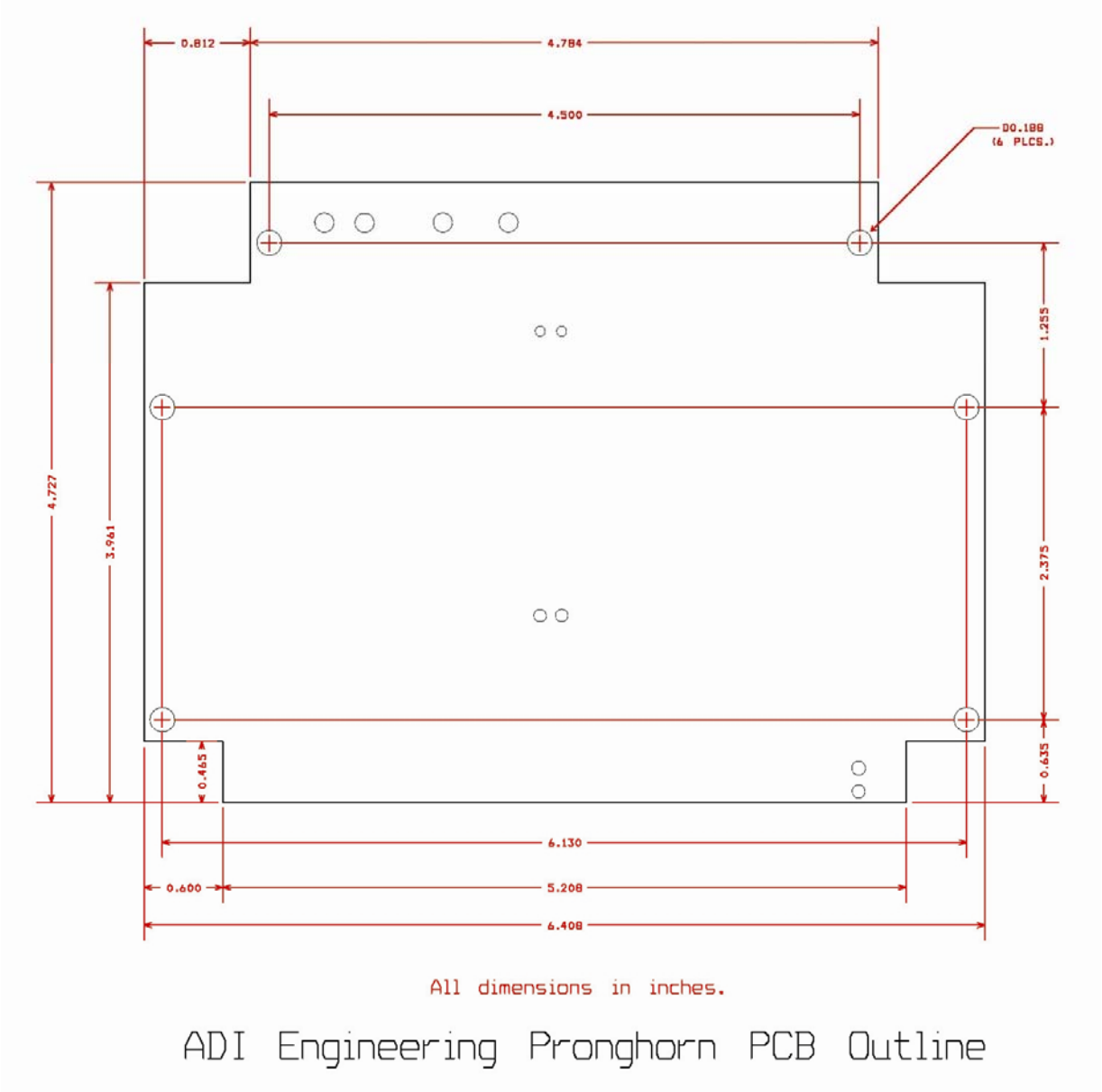

Figure 4: Pronghorn SBC Mechanical Outline

3 Appendix A – What Is Shipped?

The following table lists the various components associated with the Pronghorn SBC board. ADI offers a Pronghorn Development Kit including all the items so indicated in the following table.

Table 10. Pronghorn SBC Component List

Item	Qty	Component (Vendor, Description, Part#)	Development Kit (sold separately)
1	1	Pronghorn SBC Board w/Redboot boot monitor installed Note: Boards purchased from distributors or 3rd parties may have other software installed.	
2	1	DB9-to-RJ45 Serial adapter (SBC250 and 210 only) Vendor: Belkin Description: DB9F TO RJ45F MODULAR ADAPTER KIT Item#: F4C170 http://www.belkin.com/	Included
3	1	RS232 TTL Adapter cable (SBC200 and ELC only) Vendor: SuperDroidRobots Vendor: RS232 3.3V TTL 72inch Type 1 Serial Converter Cable Item#: MCU-026-172 http://www.superdroidrobots.com/	Included
4	1	5VDC Power supply Vendor: Digikey Description: 5VDC brick-style power supply Part#: T377-P5P-ND http://www.digikey.com/	Included
5	3	Ethernet drop cable Vendor: Belkin Description: RJ45 CAT-5e Patch Cable, Snagless Molded Yellow 06 Part#: A3L791-06-YLW http://www.belkin.com/	Included
6	1	Compact Flash card Vendor: Any	
7	1-2	MiniPCI radio cards Vendor: Any	